IN THE CLAIMS

This listing of claims replaces all prior versions and listings of the claims in the above-referenced application.

1. (Currently Amended) A device comprising:

a semiconductor light emitting device comprising:

an n-type layer;

a p-type layer;

an active region interposing the n-type layer and the p-type layer;

an n-contact electrically connected to the n-type layer; and

a p-contact electrically connected to the p-type layer;

wherein the n- and p-contacts are formed on a same side of the semiconductor light emitting device; and

a submount comprising:

first and second conductive regions on a first side of the submount; ~~and~~

third and fourth conductive regions on a second side of the submount;

a semiconductor region; and

an insulating region, wherein the n- and p-contacts of the semiconductor light emitting device are electrically and physically connected to the first and second conductive regions of the submount in a flip chip configuration.

2. (Original) The device of claim 1 wherein the first and second conductive regions comprise a material selected from the group consisting of gold, silver, nickel, platinum, and copper.

3. (Original) The device of claim 1 wherein the first and third conductive regions are electrically connected by a first conductive layer and the second and fourth conductive regions are electrically connected by a second conductive layer.

4. (Original) The device of claim 3 wherein the first and second conductive layers are metal layers.

5. (Original) The device of claim 3 wherein the first and second conductive layers are highly doped semiconductor layers.

6. (Original) The device of claim 3 wherein the first and second conductive layers are disposed on the outside of the submount.

PATENT LAW GROUP LLP
2635 N. FIRST ST.
SUITE 223
SAN JOSE, CA 95134
(408) 382-0480
FAX (408) 382-0481

7. (Original) The device of claim 3 wherein the first and second conductive layers are disposed within the submount.

8. (Original) The device of claim 7 wherein the first and second conductive layers each at least partially surround a region of semiconductor material within the submount.

9. (Original) The device of claim 7 wherein the first and second conductive layers comprise copper.

10. (Original) The device of claim 1 wherein the semiconductor light emitting device is mounted in a well formed on the submount.

11. (Original) The device of claim 10 wherein at least a portion of the sides and bottom of the well are reflective to light emitted by the semiconductor light emitting device.

12. (Original) The device of claim 10 wherein the well is at least partially filled with an optical coupling material.

13. (Canceled).

14. (Currently Amended) The device of claim ~~13~~ further comprising circuitry formed in the semiconductor region.

15. (Currently Amended) The device of claim ~~13~~ wherein the ~~non-semiconductor~~ insulating region comprises glass.

16. (Original) The device of claim 1 further comprising:

a board; and

a solder joint connecting the board to the third and fourth conductive regions.

17. (Original) The device of claim 1 wherein the semiconductor light emitting device has an area greater than about 400 x 400 μm^2.

18. (Original) The device of claim 1 wherein the semiconductor light emitting device is capable of operating at a current density of at least $50A/cm^2$.

19. (Original) The device of claim 1 wherein the semiconductor light emitting device has an area greater than or equal to about 1x1 mm^2.

20. (Original) The device of claim 1 wherein the semiconductor light emitting device is capable of operating at an electrical power consumption greater than or equal to 1W.

21. (Original) The device of claim 1 wherein a surface of the submount including the first and second conductive regions is free of wire-bond pads.

22. (Original) The device of claim 1 further comprising a luminescent material layer overlying a surface of the semiconductor light emitting device opposite the submount.

PATENT LAW GROUP LLP
2635 N. FIRST ST.
SUITE 223
SAN JOSE, CA 95134
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FAX (408) 382-0481

23. (Original) The device of claim 22 wherein the luminescent material layer overlies a side surface of the semiconductor light emitting device.

24. (Original) The device of claim 1 wherein the first, second, third, and fourth conductive regions each comprise solderable layers.

25. (Original) The device of claim 1 wherein the semiconductor light emitting device has an area less than about 400 x 400 μm^2.

26. (Original) The device of claim 1 wherein the semiconductor light emitting device is capable of operating at a current between about 5 mA and about 100 mA.

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GROUP LLP
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FAX (408) 382-0481